REMARKS

In view of the foregoing amendments and the following remarks, reconsideration and allowance of this application is requested. Claims 1-2, 4-9, 15, and 22-23 are now pending, with claim 1 being independent. The Examiner in paragraph 1 of his Office Action mailed July 16, 2003 states that "[a]fter further review, the Examiner agrees with the Applicant that claim 1 is generic to claim 2-31." As discussed with the Examiner by telephone on December 30, 2003, upon allowance of generic claim 1, dependent claims 2-31 will also be allowed because these claims are dependent to claim 1 or otherwise include all the limitations of generic claim 1 (see 37 CFR 1.141(a)).

Claim 1 has been amended to clarify the meaning of the phrase "a planar outer surface." This amendment is made for clarification purposes only and is not intended to alter the scope of the claims. No new matter has been introduced.

As amended, claim 1 presents a semiconductor device that includes a semiconductor chip with a planar active surface. The planar active surface has an integrated circuit protected by an inorganic overcoat, the integrated circuit having metallization patterns with a plurality of contact pads. As shown in Figure 2, each of the contact pads 202 has an added conductive layer 205 on the metallization patterns. The added conductive layer 205 has a conformal surface adjacent the semiconductor chip that includes peripheral portions 205a of the inorganic overcoat 203. The added conductive layer 205 also has a planar outer surface 206, 207 defining a flat outline, the planar outer surface suitable to form metallurgical bonds without melting.

Independent claim 1 stands rejected under 35 U.S.C. § 103(a) as obvious over Lin et al. (6,426,281). Applicants request reconsideration and withdrawal of this rejection for at least the reason that Lin does not describe or suggest that the added conductive layer has a planar outer surface defining a flat outline.

Lin describes a method to form solder bumps on the surface of semiconductor devices. Lin's method performs a series of processing steps including depositing and patterning a layer of passivation 34 over a contact pad 32 as shown in Figure 16. Patterning creates an opening in the layer of passivation 34 that aligns with the contact pad 32. A conductive layer of Under Ball Metallurgy (UBM) metal 36 is deposited over the layer of passivation 34 and contact pad 32. The central surface of the layer of UBM is electroplated with a copper layer 46 and a titanium layer 48 on top of the copper layer 46 as shown in Figure 16. After these steps, a layer of solder

is placed over the electroplated surfaces 46, 48 of the layer of UBM. Flowing of the layer of solder creates the solder bump 50 shown in Figure 17 of the invention. As shown in Figures 16 and 17, the outer surface of the semiconductor device contains a ridged UBM conductive layer 36 and curved solder bump 50. Thus, Lin does not describe or suggest that the added conductive layer has a planar outer surface defining a flat outline but rather a surface with ridges and curves.

The planar outer surface defining a flat outline for the added conductive layer provides several advantages. In particular, the flat outline of the planar outer surface around the contact pad reduces stress and cracking along the bond with the terminal pads of the wiring board, resulting in improved reliability of the device.

For at least the reasons given above, Applicants respectfully submit that claim 1 is patentable over Lin.

Amended claim 2 further recites that the planar outer surface defining a flat outline presented in claim 1 is substantially parallel to the chip surface.

Claim 2 stands rejected under 35 U.S.C. § 103(a) as obvious over Lin et al. (6,426,281) in view of Kleffner et al. (5,943,597). However, Kleffner fails to remedy the failure of Lin to describe or suggest that the added conductive layer has a planar outer surface defining a flat outline. Kleffner also does not describe or suggest that the flat outline is substantially parallel to the chip surface. Kleffner describes use of a trench for stress relief in a bumped semiconductor device as shown in Figure 2. The bumped semiconductor device includes a bond pad 12 formed on a semiconductor die 10. A solder bump 22 is formed so as to overlie the bond pad 12 through a UBM conductive layer 18. A stress isolation trench 15 is formed in a passivation layer 14, so as to surround the solder bump 22. Kleffner does not describe or suggest that the conductive layer 18 has a planar outer surface defining a flat outline substantially parallel to the chip surface but rather a curved surface because of the solder bump 22. Accordingly, Applicants request reconsideration and withdrawal of the rejection for at least the reasons discussed above and with respect to claim 1.

Claims 4-9 and 15 depend from independent claim 1. Accordingly, Applicants request reconsideration and withdrawal of the rejections for claims 4-9 and 15 for at least the reasons discussed above with respect to claim 1.

Claims 22 and 23 stand rejected under 35 U.S.C. § 103(a) as obvious over Lin et al. (6,426,281) in view of Elenius et al. (6,287,893). However, Elenius fails to remedy the failure of

Lin to describe or suggest that the added conductive layer has a planar outer surface defining a flat outline. Elenius describes, as shown in Figure 2, a chip scale package 8 for a flip chip integrated circuit 10 that includes a redistribution conductive layer 30 upon the upper surface of a semiconductor wafer 14 for simultaneously attaching to solder balls 28 as well as with the conductive bond pad 18 of the underlying integrated circuit. Elenius does not describe or suggest that the conductive layer 30 has a planar outer surface defining a flat outline but rather an outer surface interrupted by a large sphere-like solder ball as shown in Figures 2 and 3 for attachment to a circuit board. Accordingly, Applicants request reconsideration and withdrawal of the rejection for at least the reasons discussed above and with respect to claim 1.

In view of these remarks and amendments, the Applicants submit that this application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

Date: 12/30/2003

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